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FIG. 1

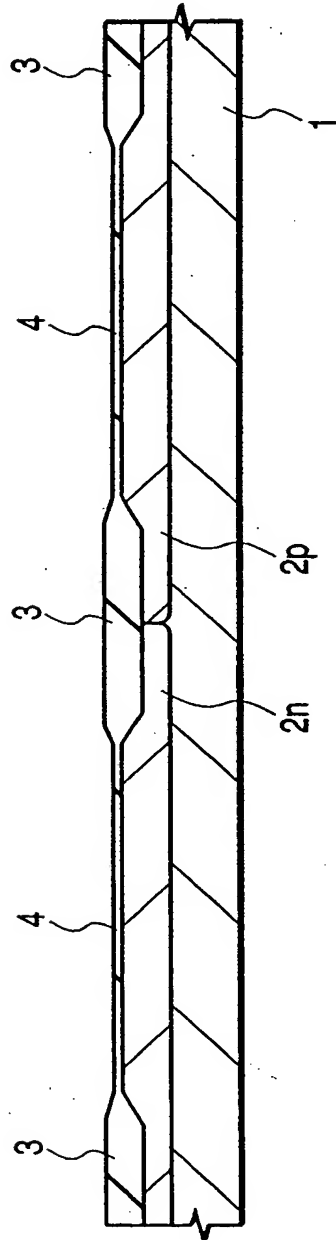
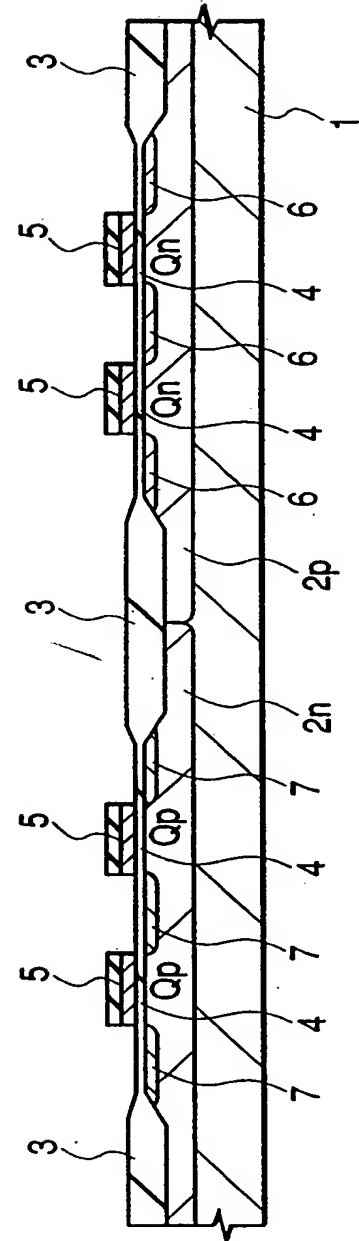


FIG. 2



This diagram shows a cross-sectional view of a semiconductor device. It features a substrate with a series of layers and regions. The layers are labeled with numbers 1 through 21. The regions are labeled with letters Qn, Qp, and 2p. The device includes a central channel region (3) and a gate region (5). The gate region is formed by a series of overlapping layers (12, 13, 14, 15, 16, 17, 18, 19, 20, 21) and a gate oxide layer (11). The channel region (3) is formed by a series of overlapping layers (3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19, 20, 21) and a channel oxide layer (Qn, Qp). The device is shown in a cross-sectional view, with the layers and regions labeled with numbers and letters.

FIG. 7

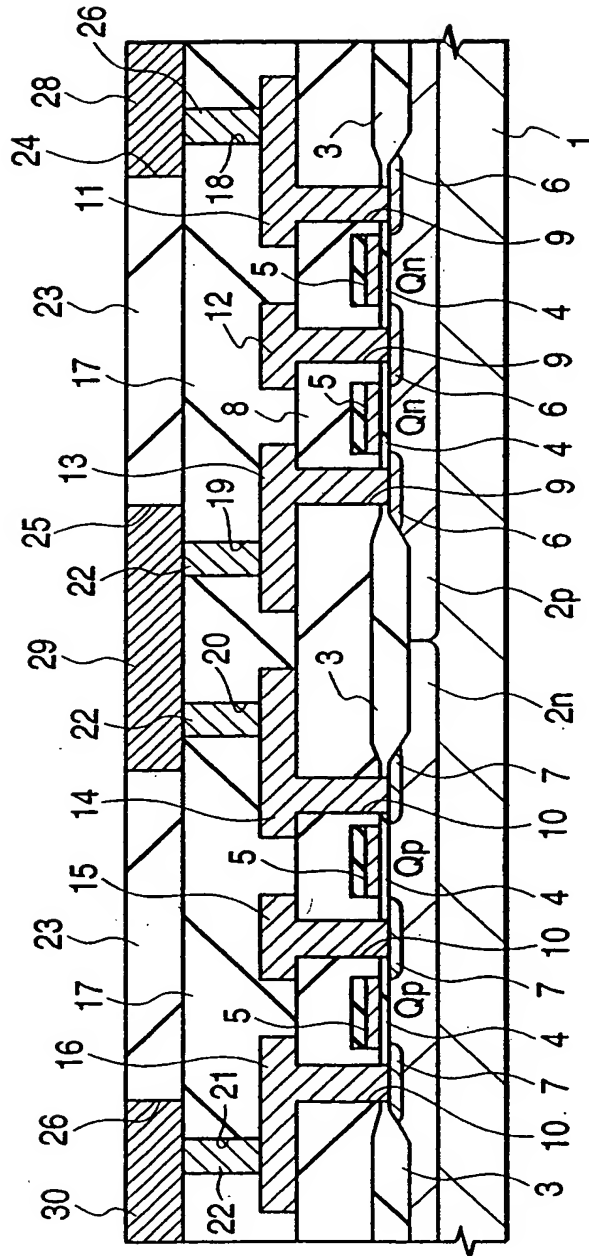


FIG. 8

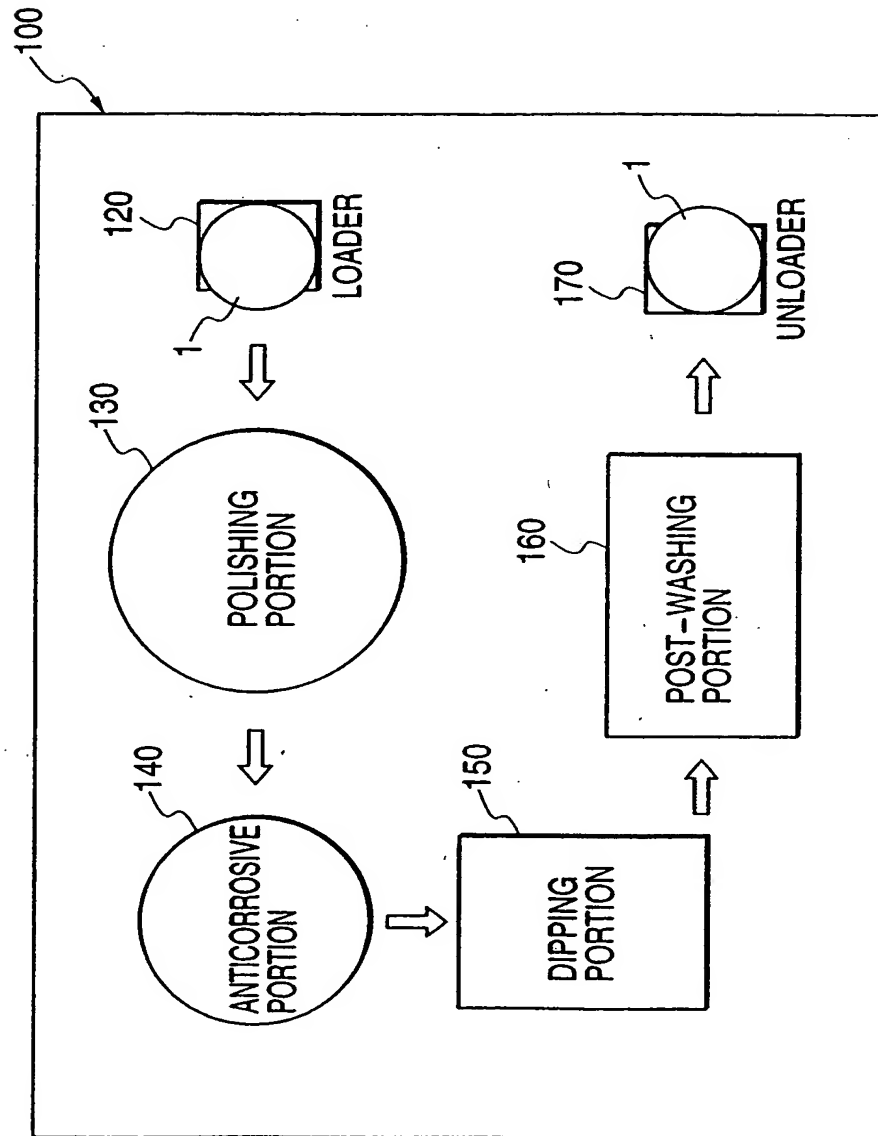


FIG. 9

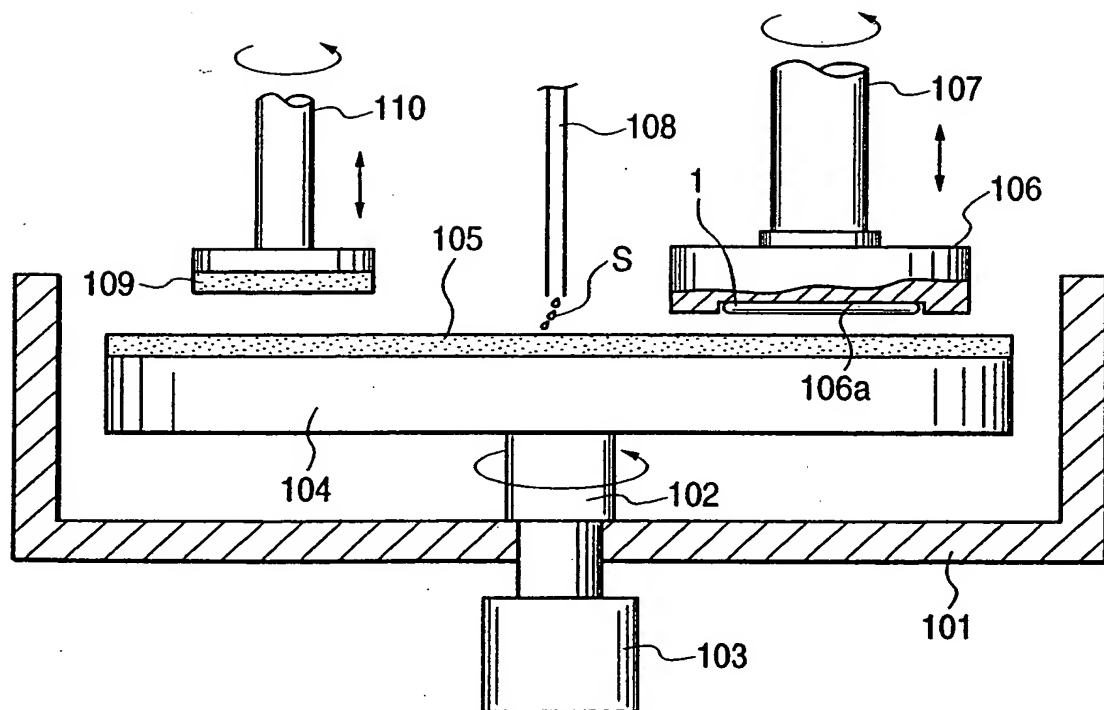


FIG. 10

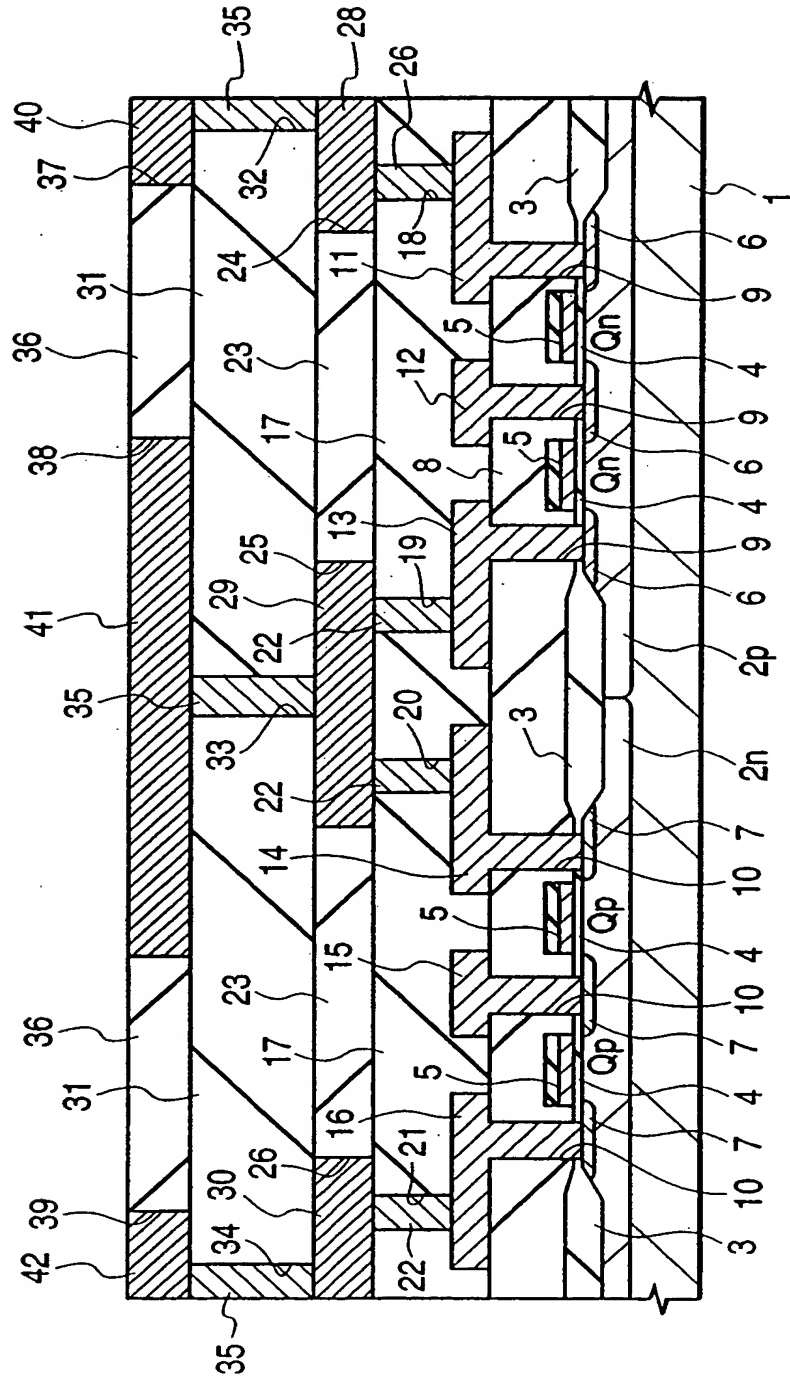


FIG. 11

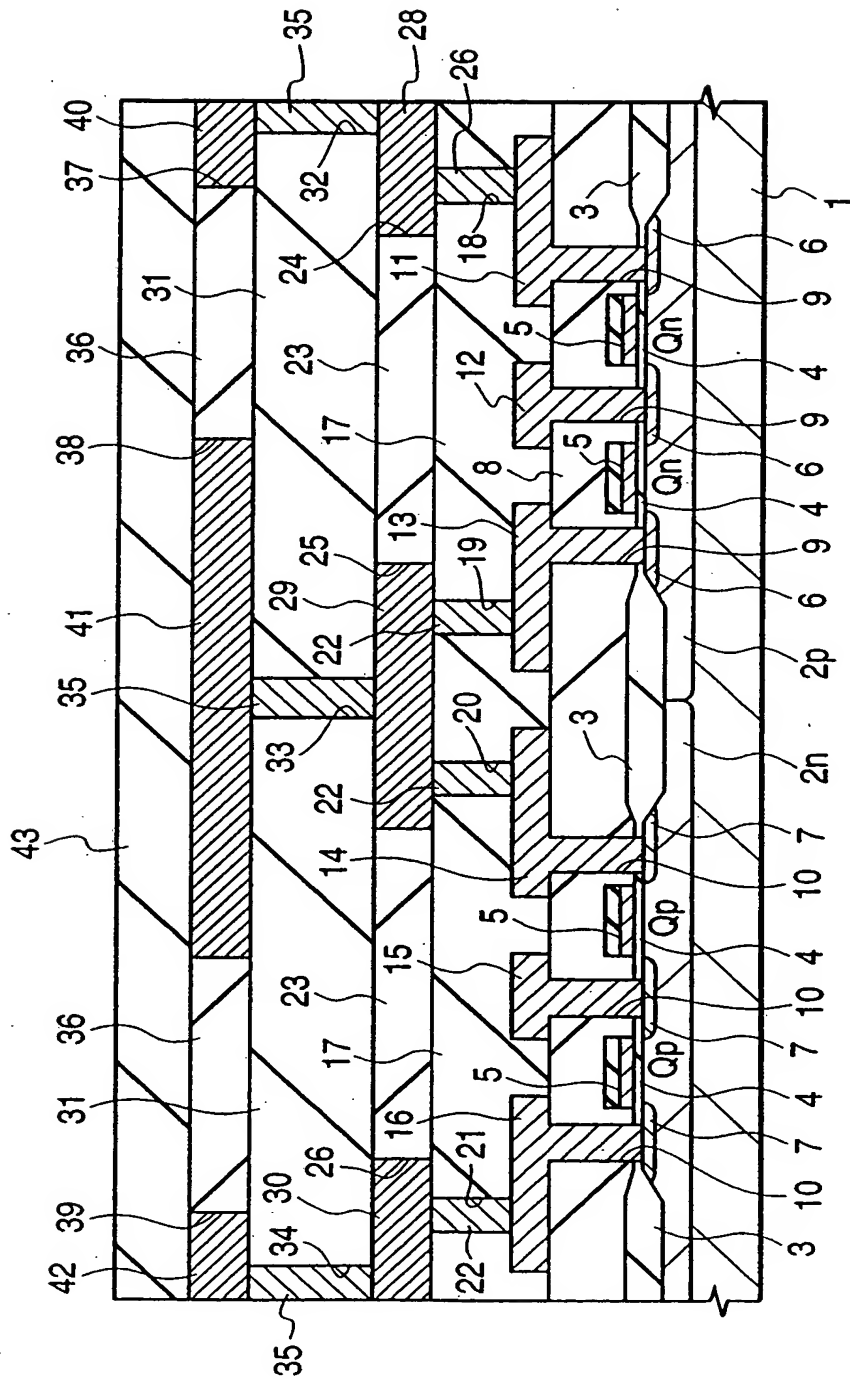


FIG. 12

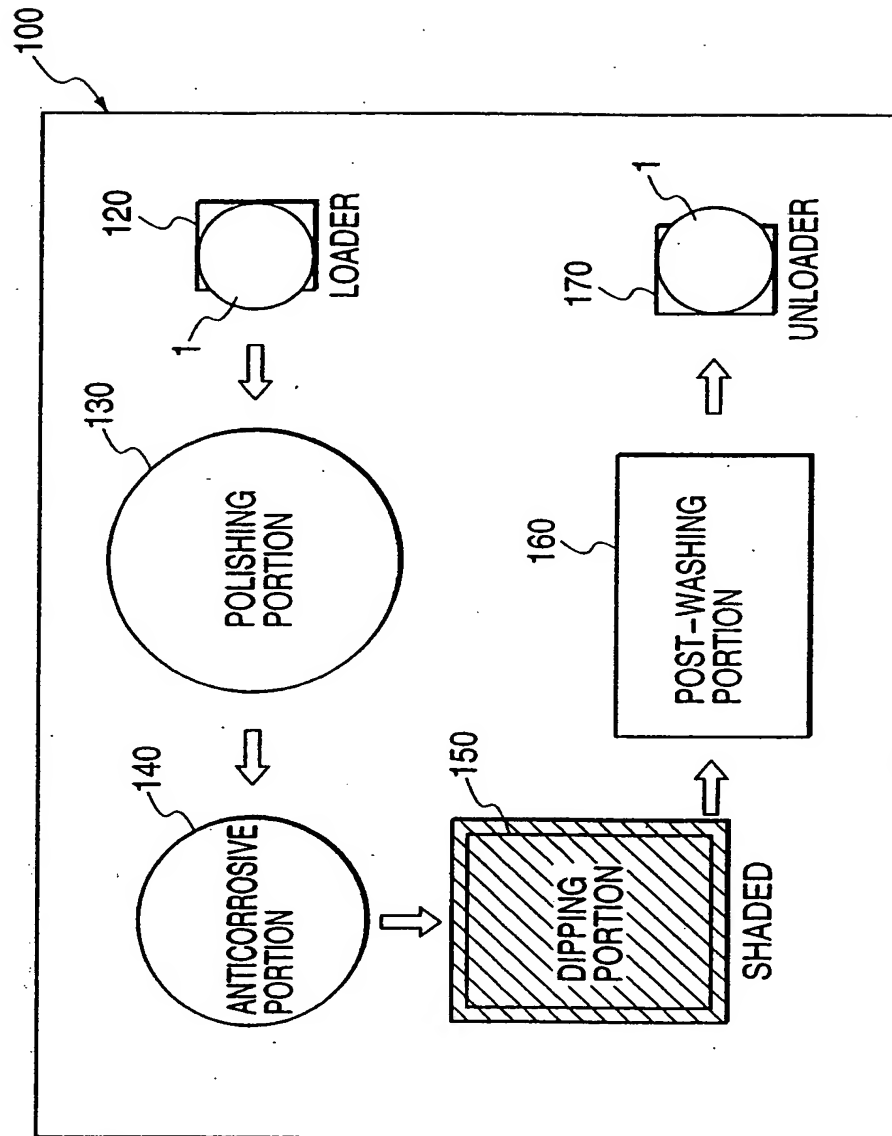


FIG. 13

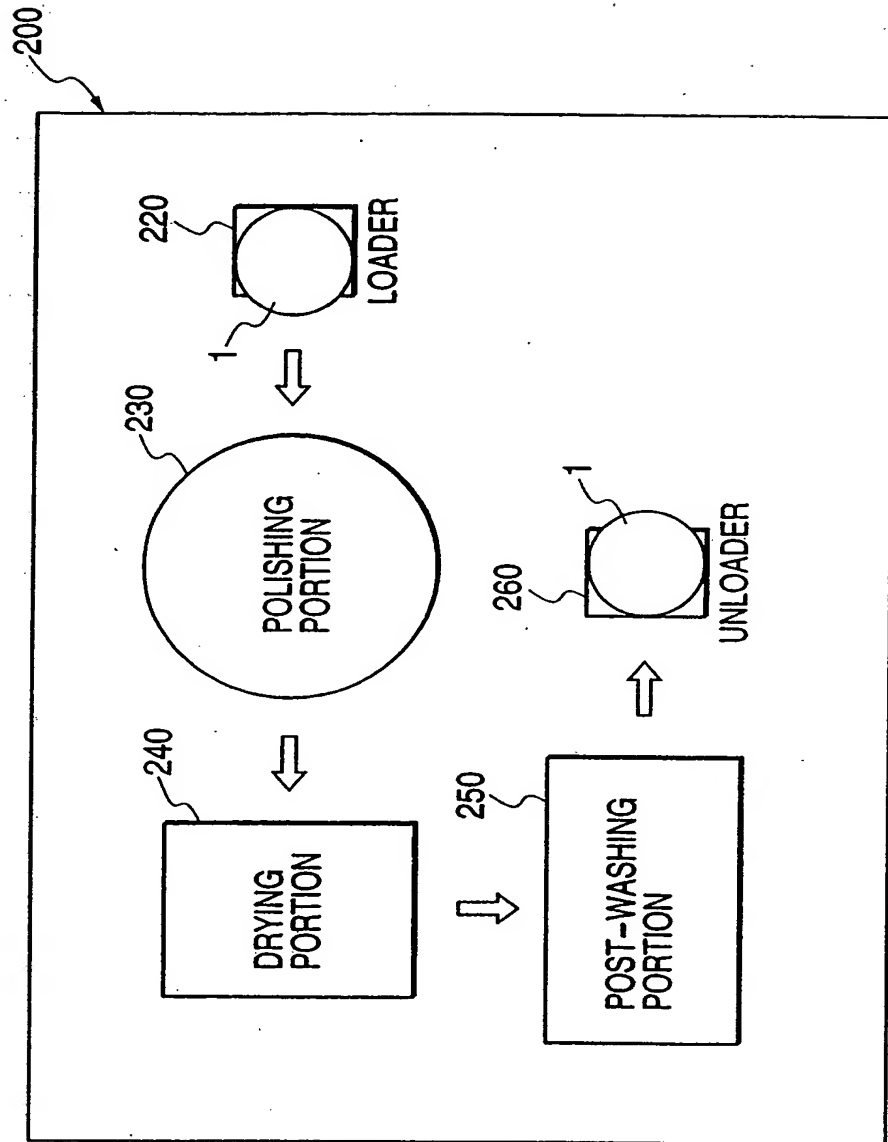


FIG. 14(a)

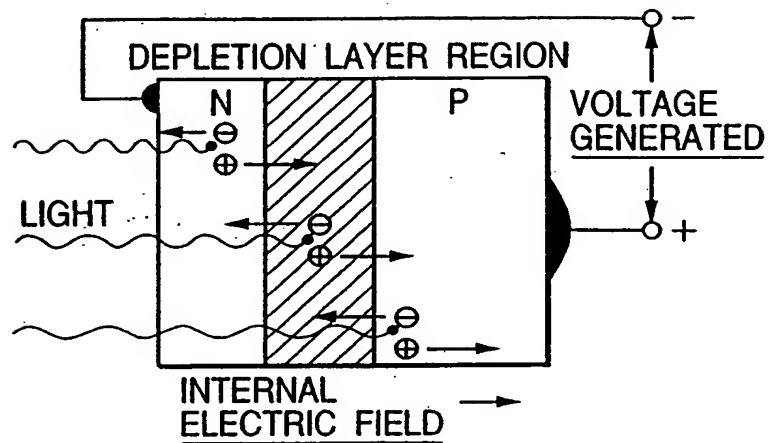


FIG. 14(b)

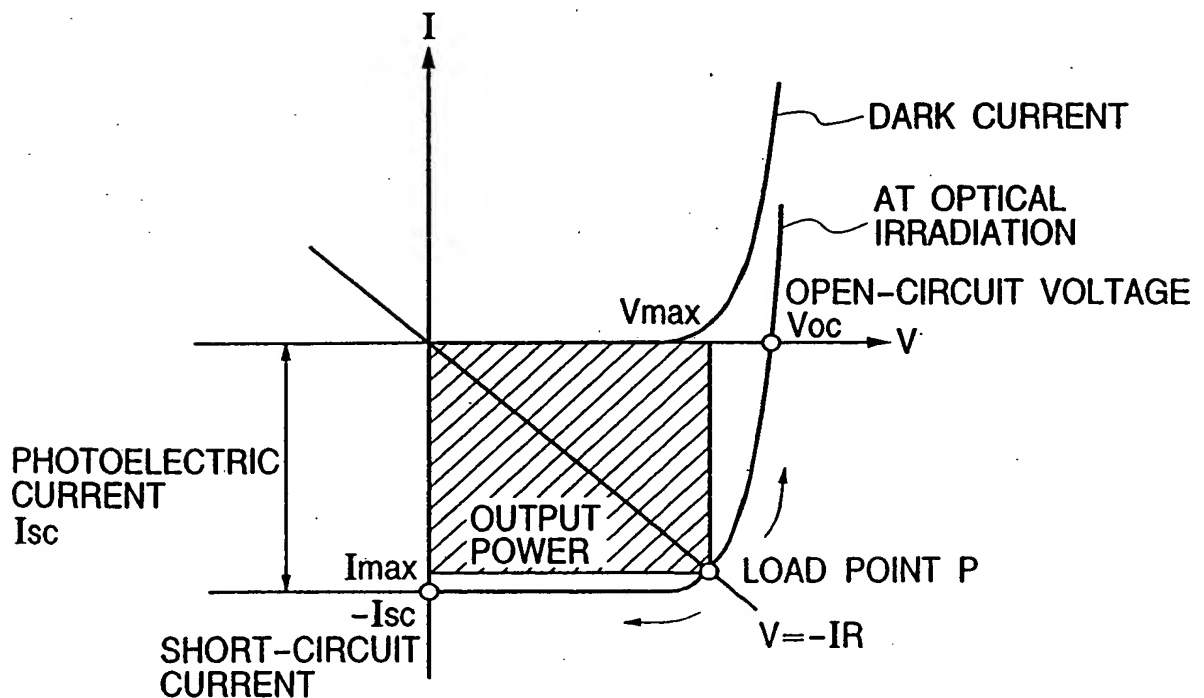


FIG. 15

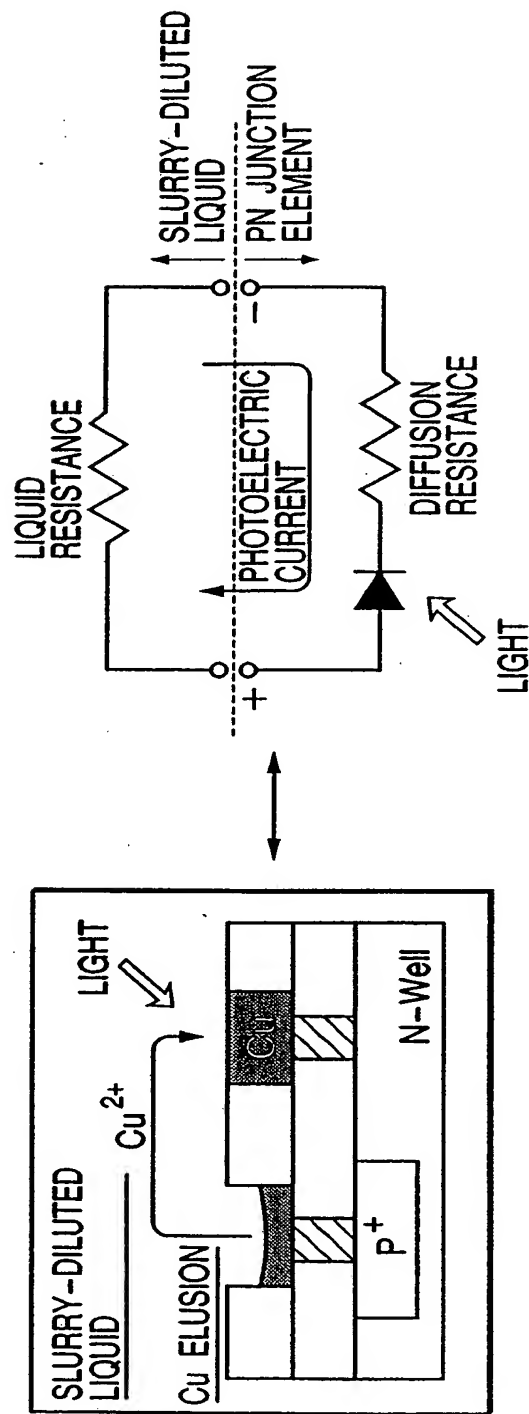


FIG. 16

